Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-68. (canceled)

69. (previously presented) A semiconductor chip or wafer comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate;

a passivation layer over said interconnecting metallization structure, wherein an opening in said passivation layer exposes a contact point of said interconnecting metallization structure;

a first metal layer over said contact point, wherein said first metal layer comprises aluminum; and

a second metal layer over said first metal layer, wherein said second metal layer is used to be wirebonded thereto.

70. (previously presented) The semiconductor chip or wafer of claim 69, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

71. (previously presented) The semiconductor chip or wafer of claim 69, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

72. (previously presented) The semiconductor chip or wafer of claim 69, wherein said interconnecting metallization structure comprises copper.

73. (previously presented) The semiconductor chip or wafer of claim 69, wherein said second metal layer comprises gold.

74. (previously presented) The semiconductor chip or wafer of claim 69, wherein said second metal layer comprises copper.

75. (previously presented) The semiconductor chip or wafer of claim 69, wherein said second metal layer has a thickness of between about 2μm and 20μm.

76. (previously presented) The semiconductor chip or wafer of claim 69 further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises a titanium-tungsten alloy.

77. (previously presented) The semiconductor chip or wafer of claim 69 further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises chromium.

78. (previously presented) The semiconductor chip or wafer of claim 69 further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises titanium.

79. (previously presented) The semiconductor chip or wafer of claim 69 further comprising a third metal layer between said first and second layers, wherein said third metal layer has a thickness of between 2700 and 3300 Angstroms.

80. (new) A semiconductor chip or wafer comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate;

a passivation layer over said interconnecting metallization structure, wherein an opening in said passivation layer exposes a contact point of said interconnecting metallization structure;

a first metal layer over said contact point, wherein said first metal layer comprises aluminum;

a second metal layer over said first metal layer; and

a wire wirebonded over said second metal layer.

81. (new) The semiconductor chip or wafer of claim 80, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

82. (new) The semiconductor chip or wafer of claim 80, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

83. (new) The semiconductor chip or wafer of claim 80, wherein said interconnecting metallization structure comprises copper.

84. (new) The semiconductor chip or wafer of claim 80, wherein said second metal layer comprises gold.

85. (new) The semiconductor chip or wafer of claim 80, wherein said second metal layer comprises copper.

86. (new) The semiconductor chip or wafer of claim 80, wherein said second metal layer has a thickness of between about 2μm and 20μm.

87. (new) The semiconductor chip or wafer of claim 80 further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises a titanium-tungsten alloy.

88. (new) The semiconductor chip or wafer of claim 80 further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises chromium.

89. (new) The semiconductor chip or wafer of claim 80 further comprising a third metal layer between said first and second layers, wherein said third metal layer comprises titanium.

90. (new) The semiconductor chip or wafer of claim 80 further comprising a third metal layer between said first and second layers, wherein said third metal layer has a thickness of between 2700 and 3300 Angstroms.